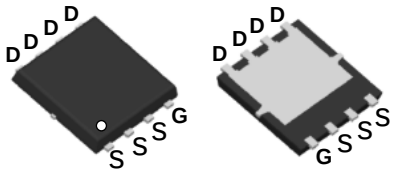
WMB129N10T2

100V N-Channel Enhancement Mode Power MOSFET

Description

WMB129N10T2 uses advanced power trench technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

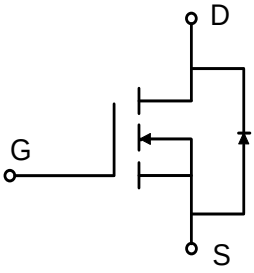


PDFN5060-8L

Features

- V_{DS} = 100 V, I_D = 129A（Silicon Limited）
  $R_{DS(on)}$ < 4.2mΩ @ V_{GS} = 10V
  $R_{DS(on)}$ < 6mΩ @ V_{GS} = 4.5V
- Green Device Available
- 100% EAS Guaranteed
- Optimized for High Speed Smooth Switching

RoHS compliant



Applications

- Power Management Switches
- DC/DC Converter

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current[1]（Silicon Limited）	T_C=25℃	I_D	129	A
	T_C=100℃		80	
Continuous Drain Current[1](Package Limited)	T_C=25℃		60	
Pulsed Drain Current[2]		I_{DM}	402	A
Single Pulse Avalanche Energy[3]		EAS	101.2	mJ
Avalanche Current		I_{AS}	45	A
Total Power Dissipation[4]	T_C=25℃	P_D	127.5	W
Operating Junction and Storage Temperature Range		T_J , T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient[1]	$R_{\theta JA}$	49	°C/W
Thermal Resistance from Junction-to-Case[1]	$R_{\theta JC}$	0.98	°C/W

Electrical Characteristics T_c = 25°C, unless otherwise noted

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	100	-	-	V
Gate-body Leakage Current		I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T_J=25℃	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V	-	-	1	μA
	T_J=100℃			-	-	100	
Gate-Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.4	1.8	2.4	V
Drain-Source On-Resistance[2]		$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A	-	3.5	4.2	mΩ
			V_{GS} = 4.5V, I_D = 20A	-	4.8	6	
Forward Transconductance[2]		g_{fs}	V_{DS} = 5V, I_D = 20A	-	81	-	S
Dynamic Characteristics							
Input Capacitance		C_{iss}	V_{DS} = 50V, V_{GS} =0V, f =1MHz	-	3875	-	pF
Output Capacitance		C_{oss}		-	920	-	
Reverse Transfer Capacitance		C_{rss}		-	41	-	
Switching Characteristics							
Gate Resistance		R_g	V_{DS} = 0V, V_{GS} =0V, f =1MHz	-	1.2	-	Ω
Total Gate Charge		Q_g	V_{GS} = 4.5V, V_{DD} = 50V, I_D= 20A	-	52	-	nC
Total Gate Charge		Q_g	V_{GS} = 10V, V_{DS} = 50V, I_D= 20A	-	91	-	
Gate-Source Charge		Q_{gs}		-	7.9	-	
Gate-Drain Charge		Q_{gd}		-	31.5	-	
Turn-On Delay Time		$t_{d(on)}$	V_{GS} =10V, V_{DS} = 50V, R_G = 10Ω, I_D= 20A	-	15.3	-	nS
Rise Time		t_r		-	17.8	-	
Turn-Off Delay Time		$t_{d(off)}$		-	52.4	-	
Fall Time		t_f		-	23.6	-	
Drain-Source Body Diode Characteristics							
Diode Forward Voltage[2]		V_{SD}	I_S = 20A, V_{GS} = 0V	-	-	1.2	V
Continuous Source Current[1,5]		I_S	V_G=V_D=0V , Force Current	-	-	129	A
Reverse Recovery Time		t_{rr}	V_R =50V, I_F=20A, dI_F/dt=500A/μs	-	44	-	ns
Reverse Recovery Charge		Q_{rr}		-	212	-	nC

Notes:

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%

3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=45A

4.The power dissipation is limited by 150℃ junction temperature

5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

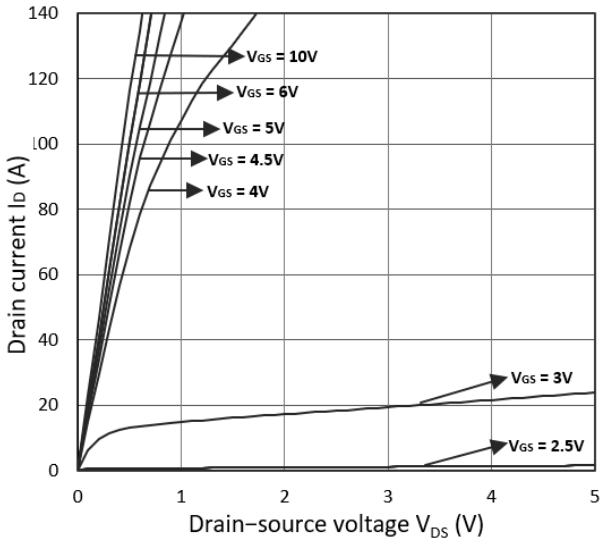


Figure 1. Output Characteristics

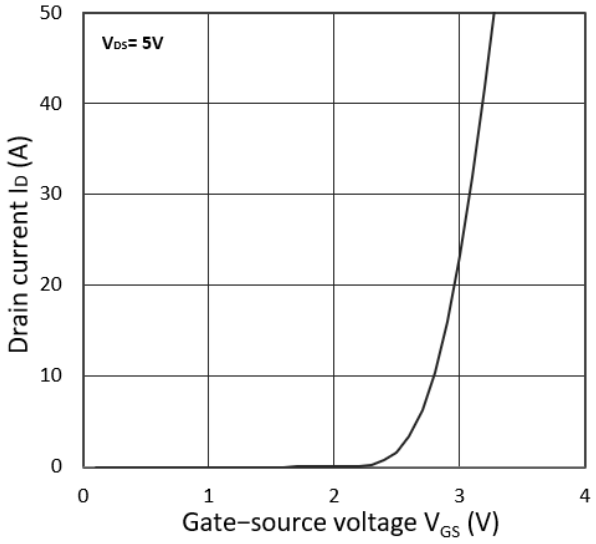


Figure 2. Transfer Characteristics

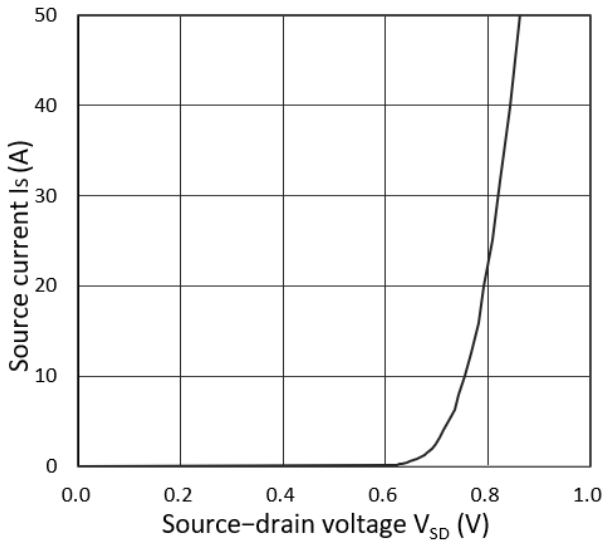


Figure 3. Forward Characteristics of Reverse

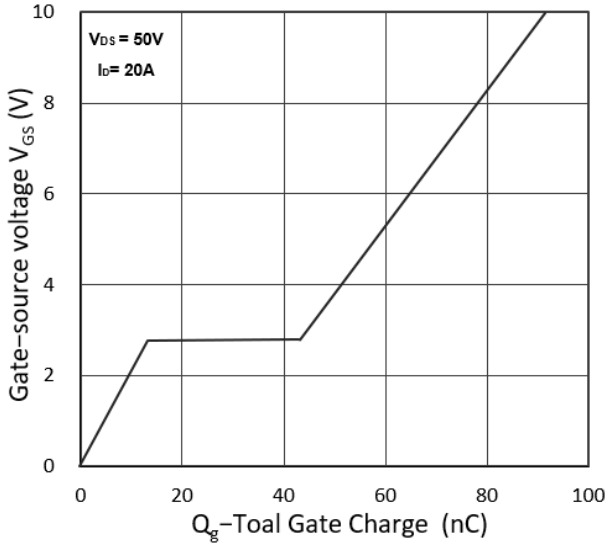


Figure 4. Gate Charge Characteristics

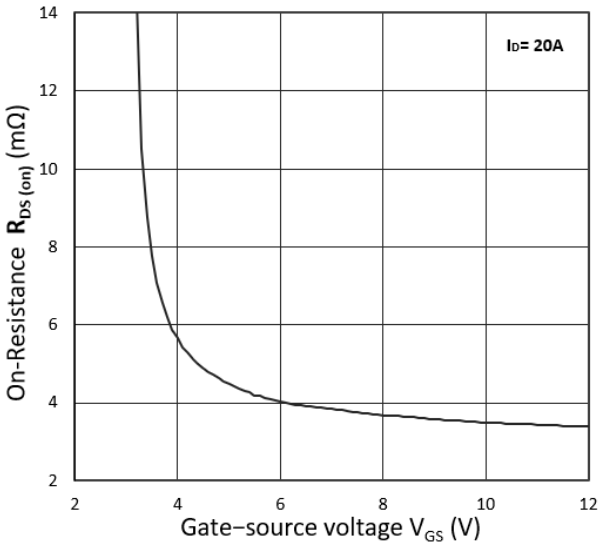


Figure 5. $R_{DS(on)}$ vs. V_{GS}

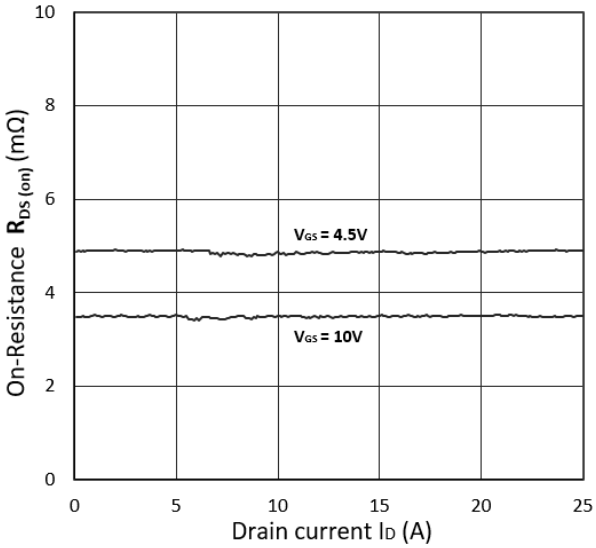


Figure 6. $R_{DS(ON)}$ vs. I_D

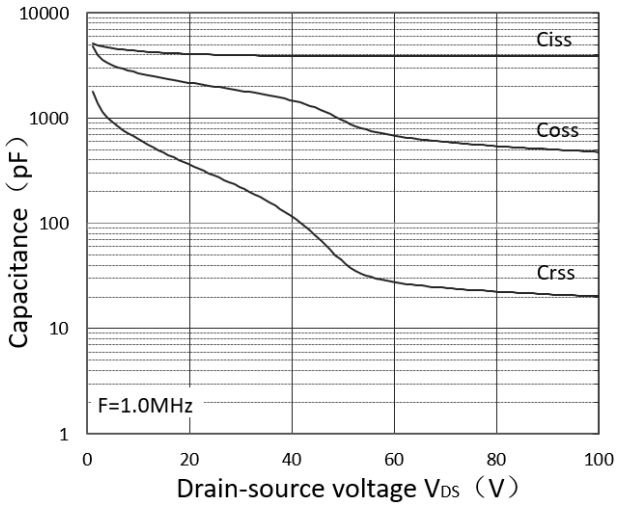


Figure 7. Capacitance Characteristics

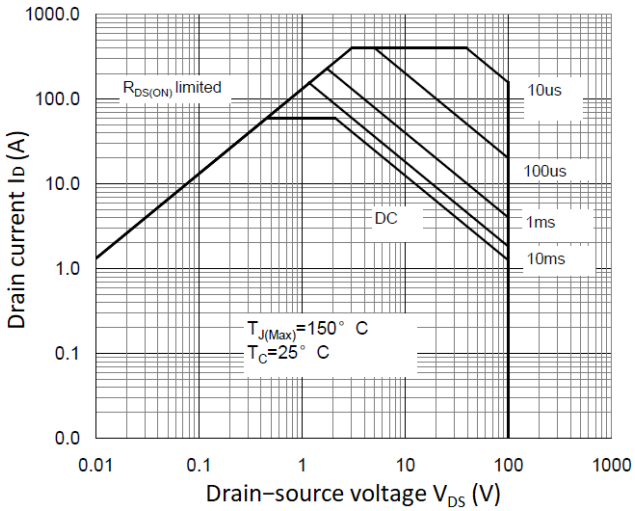


Figure 8. Safe Operating Area

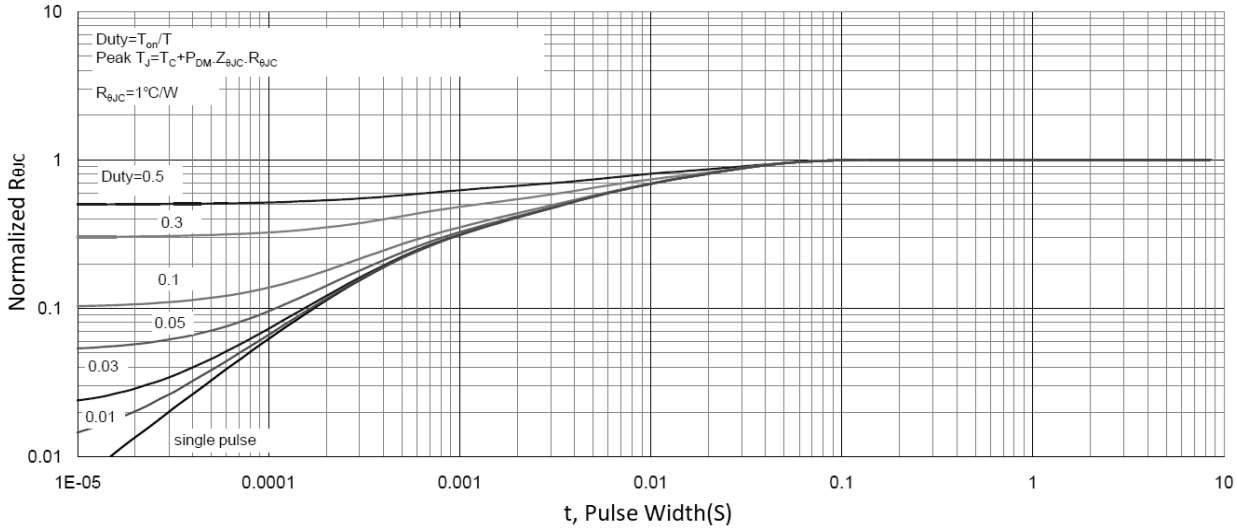


Figure 9. Normalized Maximum Transient Thermal Impedance

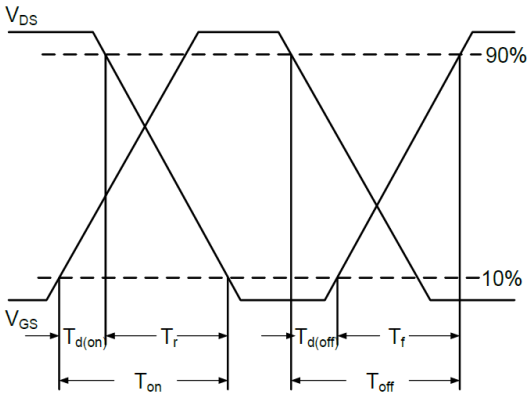


Figure 10. Switching Time Waveform

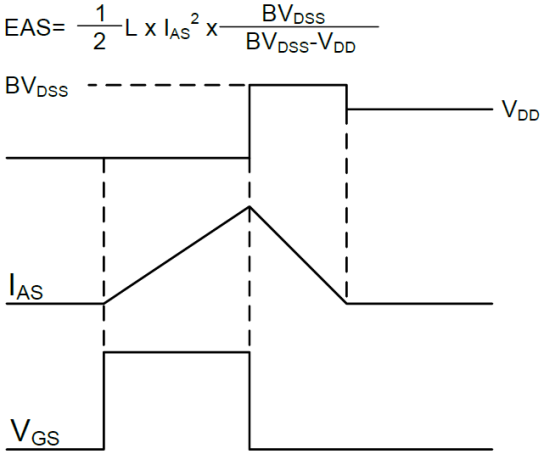
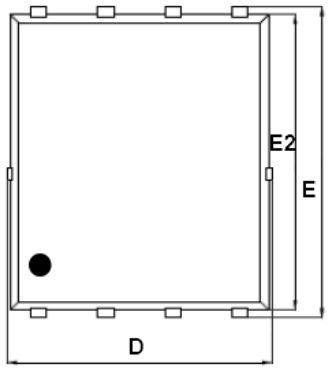
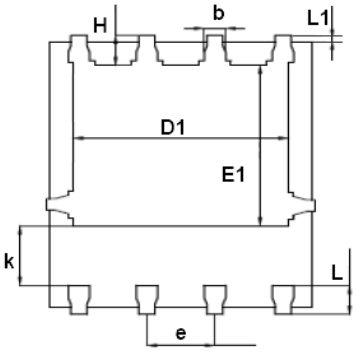


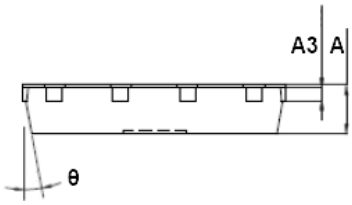
Figure 11. Unclamped Inductive Switching Waveform

Mechanical Dimensions for PDFN5060-8L

COMMON DIMENSIONS





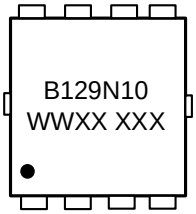


SYMBOL	MM	
	MIN	MAX
A	0.90	1.20
A3	0.15	0.35
D	4.80	5.40
E	5.90	6.35
D1	3.61	4.31
E1	3.30	3.92
E2	5.65	6.06
k	1.10	-
b	0.30	0.51
e	1.27BSC	
L	0.38	0.71
L1	0.05	0.36
H	0.38	0.61
θ	0°	12°

Ordering Information

Part	Package	Marking	Packing method
WMB129N10T2	PDFN5060-8L	B129N10	Tape and Reel

Marking Information



B129N10= Device code

WWXX XXX= Date code

Contact Information

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